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CENTRAL FAX CENTER

Application No. 09/545040 (Docket: CNTR.1568)
37 CFR 1.111 Amendment dated 01/19/2006
Reply to Office Action of 12/12/2005

JAN 20 2006

AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

To address the above-detailed deficiencies, it is an object of the present invention is to provide an apparatus for detecting and forwarding storehit data without delay that is less complex than has heretofore been provided. Accordingly, in attainment of the aforementioned object, it is a feature of the present invention to provide an apparatus for speculatively forwarding storehit data in a microprocessor pipeline. The apparatus includes first and second virtual address comparators that compare a virtual load address with first and second virtual store addresses to generate a virtual match signal for indicating whether first and second storehit data is likely present in a store buffer and a result forwarding cache, respectively, of the microprocessor. If the first and second storehit data are both present the second storehit data is newer than the first storehit data. The apparatus also includes first and second physical address comparators that compare a physical load address translated from the virtual load address with first and second physical store addresses translated from the plurality of virtual store addresses to generate a physical match signal for indicating whether the first and second storehit data is certainly present in the store buffer and the result forwarding cache, respectively. The apparatus also includes forwarding logic, coupled to receive the virtual match signal, which forwards the second storehit data present in the store buffer in response to the virtual match signal indicating no match between the virtual load address and the second virtual store addresses but a match between the virtual load address and the first virtual store address, prior to generation of the physical match signal. The apparatus also includes control logic that receives the virtual and physical match signals and generates a stall signal for stalling the pipeline subsequent to the forwarding logic forwarding the storehit data from the store buffer if the physical match signal indicates a match between the physical load address and the second physical store addresses although the virtual match signal previously indicated no match between the virtual load address and the second virtual store addresses, until correct data specified by the physical load address is provided to replace the previously forwarded second storehit data.

In yet another aspect, it is a feature of the present invention to provide a method for speculatively forwarding storehit data in a microprocessor pipeline. The method includes determining that a virtual load address matches a first virtual store addresses present in the pipeline to indicate first storehit data is likely present in a store buffer of the microprocessor, but does not match a second virtual store address present in the pipeline to indicate second newer storehit data is likely absent in a result forwarding cache of the microprocessor. The method also includes forwarding the first storehit data from a first stage comprising the store buffer to a second stage of the pipeline having a load instruction specifying the load address based on the determining that the first storehit data is likely present in the store buffer and the second newer storehit data is likely absent in

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the result forwarding cache. The method also includes detecting that a physical load address translated from the virtual load address matches a physical store address translated from the second virtual store address to indicate the second newer storehit data is certainly present in the result forwarding cache, subsequent to the forwarding the first storehit data. The method also includes stalling the pipeline in response to the detecting that the physical load address translated from the virtual load address matches the physical store address present in the pipeline, until correct data specified by the physical load address is provided to replace the previously forwarded second newer storehit data.

In yet another aspect, it is a feature of the present invention to provide a method for speculatively forwarding storehit data in a microprocessor pipeline. The method includes comparing a virtual load address with first and second virtual store addresses. A load instruction specifying the virtual load address is newer than a first store instruction specifying the first virtual store address, which is newer than a second store instruction specifying the second virtual store address. The method also includes speculatively forwarding a result of the first store instruction to the load instruction, in response to the comparing indicating the virtual load address matches the first virtual store address and mismatches the second virtual store address. The method also includes comparing a physical load address with a physical store address, wherein the physical load address is a translation of the virtual load address. The physical store address is a translation of the second virtual store address. The method also includes determining the forwarding the result of the first store instruction to the load instruction was incorrect, after the speculatively forwarding the result of the first store instruction, in response to the comparing indicating the physical load address matches the physical store address. The method also includes forwarding a result of the second store instruction to the load instruction, in response to the determining.

An advantage of the present invention is that only minimal changes are required to forward storehit data when pipeline stages are added. Another advantage of the present invention is that it realizes the timing advantages of comparing virtual addresses that are available sooner than physical addresses, in order to detect storehits, and speculatively forwarding data accordingly.